Macro Model | December 2001 | MM2541

# HA-2541
# SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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## Introduction

This application note describes the SPICE macro-model for the HA-2541, a wideband, fast settling, unity gain stable op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC paramaters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

## Model Description

### Input Stage

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is modeled with FA. Source VIO represents the input offset voltage. C1 limits slew rate. No input parasitics due to package capacitance and lead inductance are included.

### Gain Stage

G2, R2, CC, GOL, and RD simulate open loop gain. CC is the macro-model dominant pole capacitor.

### Poles and Zeros

The HA-2541 macro-model uses a complex pole and complex zero modeled with RLC networks as well as five poles and two zeros.

General poles use RC networks and zeros use RL networks. Singularity frequencies are indicated on the schematic. Instructions for converting the model to have a simple two pole response are included in the netlist. This reduces simulation time at the expense of accurate frequency response.

### Output Stage

EX1, D1 and D2 model output current limiting. IH and IL model the power supply currents. FIP and FIN vary the supply currents based on the op amps output current. DL, DH, VH and VL provide voltage clamping on the output to simulate the typical output voltage swing. No output parasitics due to package capacitance and lead inductance are included.

## Parameters Not Modeled

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

## Spice Listing

```
*
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*
* HA-2541 MACRO-MODEL
* REV: 8/8/91
*BY: D.L. YOUNGBLOOD & R.S. VOGELSONG
*
*PINOUT CHANGED TO CONFORM TO "STANDARD"
*
* PINOUT          +IN  -IN  VCC  VEE  VOUT
*
.SUBCKT  HA2541  6  7  9  10  8
.MODEL DP D      IS=1E-14          N=+1.5563E+01
.MODEL DN D      IS=+8.4545E-15    N=+1.5563E+01
.MODEL DV D      IS=1E-14          N=.5
.MODEL D1 D      IS=1E-14          N=1
.MODEL D2 D      IS=1E-14          N=+5.8815E-01
.MODEL DIO2 D    IS=1E-14          N=20
*
*INPUT STAGE
*
VP 6 12 0
DP 12 1 DP
*
*THE VALUE OF SOURCE "VIO" REPRESENTS OFFSET
*VOLTAGE AND MAY BE CHANGED TO SIMULATE WORST
*CASE, IF DESIRED
*
VIO 7 13 +4.1349E-04
*
DN 13 1 DN
FA 7 0 VIO +1.0286E-03
I1 1 0 +2.4536E-05
C1 1 0 +6.8088E-16  IC=-8.4003E+00
FP 4 0 VP  +2.2865E+02
FN 0 4 VIO  +2.7045E+02
GC 0 4 1 0 +2.4042E-07
ICO 0 4 2.0195E-6
GPP 0 4 9 48 +1.011E-07
GPN 0 4 49 10 +3.858E-07
RT 4 0 1.0
VPP 48 0 +1.5E+01
RPP 48 0 1K
VPN 0 49 +1.5E+01
RPN 0 49 1K
*
*GENERAL POLES
*
EP1 15 0 4 0 1.0
RP1 15 16 +1.10345E+01
CP1 16 0 1.0E-10
EP2 17 0 16 0 1.0
RP2 17 18 +7.6525E+00
CP2 18 0 1.0E-10
EP3 19 0 18 0 1.0
RP3 19 20 +6.5466E+00
CP3 20 0 1.0E-10
EP4 21 0 20 0 1.0
RP4 21 22 +5.7505E+00
CP4 22 0 1.0E-10
EP5 24 0 22 0 1.0
RP5 24 25 +3.1289E+00
CP5 25 0 1.0E-10
*
*GENERAL ZEROES
*
GZ1 0 30 25 0 +6.2407E-04
VZ01 30 31 0.0
RHZ1 31 32        +1.6024E+03
LZ1 32 0 1.0E-6
GZ2 0 33 30 0 +5.0672E-04
VZ02 33 34 0.0
RHZ2 34 35        +1.9735E+03
LZ2 35 0 1.0E-6
*
*COMPLEX ZERO
*
ECZ 42 0 33 0 1.0
VCZ 42 43 0.0
CC2Z 43 0 +6.9559E-13
RBIG2 43 0 1.0E+7
FCZ 0 38 VCZ      1.0
LCZ 38 39 1.0E-6
CC1Z 39 40 +6.9559E-13
RHCZ 40 0 +5.9231E+02
RBIG1 38 0 1.0E+7
*
*COMPLEX POLE
*
ECP 45 0 38 0 1.0
RCP 45 46 +5.7687E+02
LCP 46 47 +6.4195E-07
CCPX 47 0 1.0E-12
*
*GAIN/OUTPUT STAGE
*
*FOR LEVEL 1 MODEL, CHANGE NODE 47 ON SOURCE "G2"
*TO 4, ADD A CAPACITOR FROM NODE 4 TO NODE 0 OF THE
*VALUE 2.926E-9, AND COMMENT OUT ALL POLES AND ZEROS
*
G2 0 2 47 0 1.0
*
R2 2 0 +1.4769E+05
D2A 2 0 DIO2
D2B 0 2 DIO2
CC 2 3 +2.2E-11
GOL 3 0 2 0 4.7231E+01
RD 3 0 5.0000E-01
DH 3 5 DV
DL 50 3 DV
VH 9 5 4.2171
VL 50 10 2.03
IH 9 0 +3.0573E-02
IL 0 10 +3.0600E-02
D1 3 53 D1
D2 53 3 D2
EX1 53 0 POLY  2  3  0  3  8  0  1  -7.350E+00
RO 54 8 +1.5000E+00
VIS 3 54 0
FI 0 55 VIS 1
DIP 55 56 DV
DIN 58 57 DV
VIP 56 58 0
VIN 57 55 0
RI 58 0 1.0
FIP 9 0 VIP 1.0
FIN 0 10 VIN 1.0
.ENDS HA2541
```
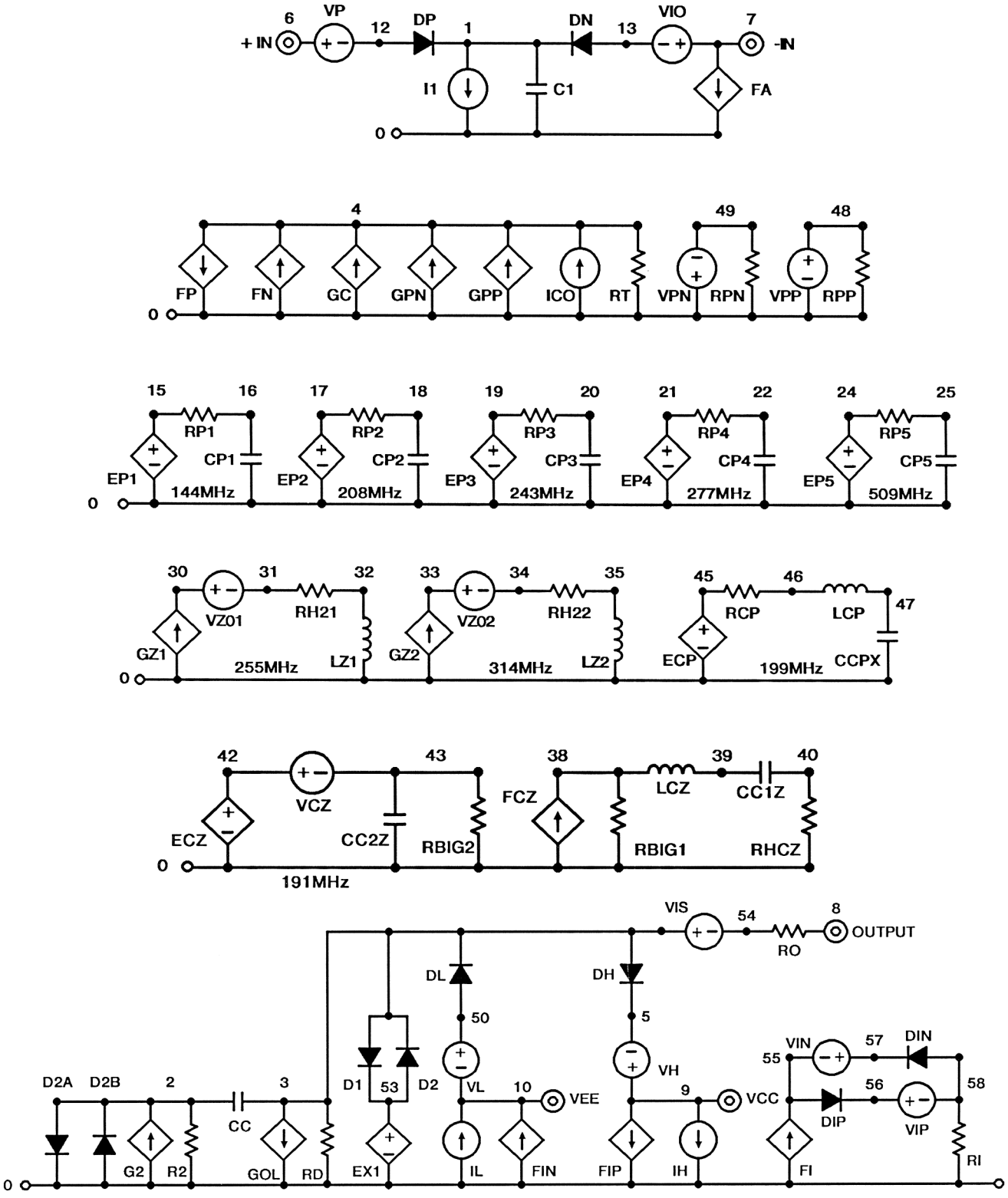
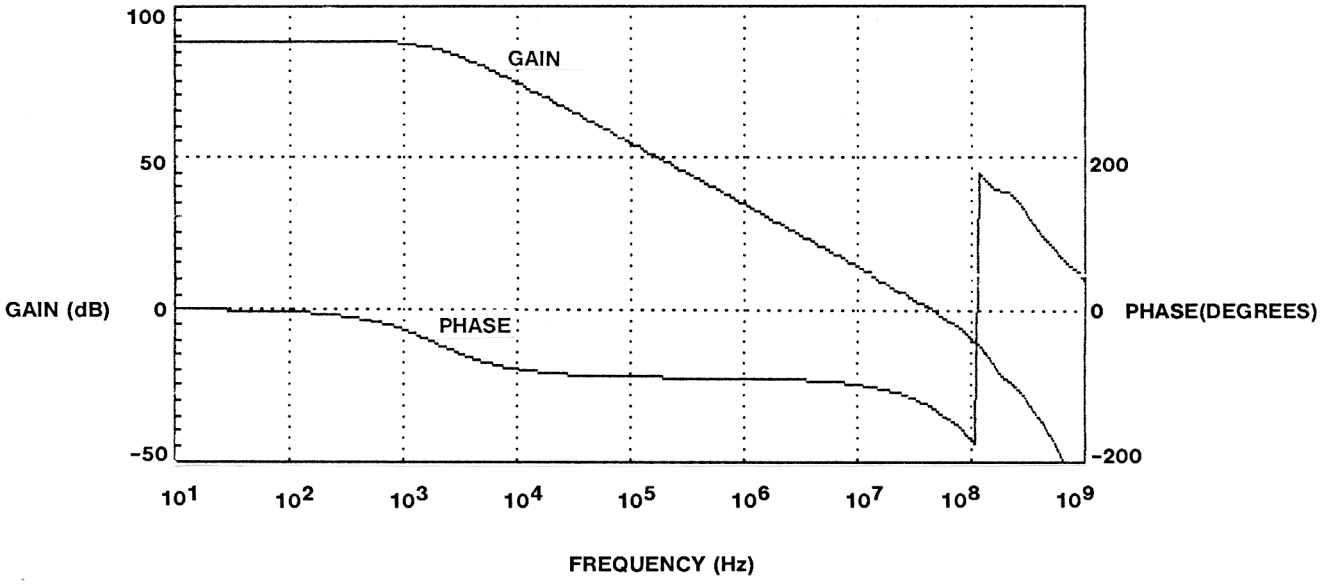

## Macro-Model Schematic

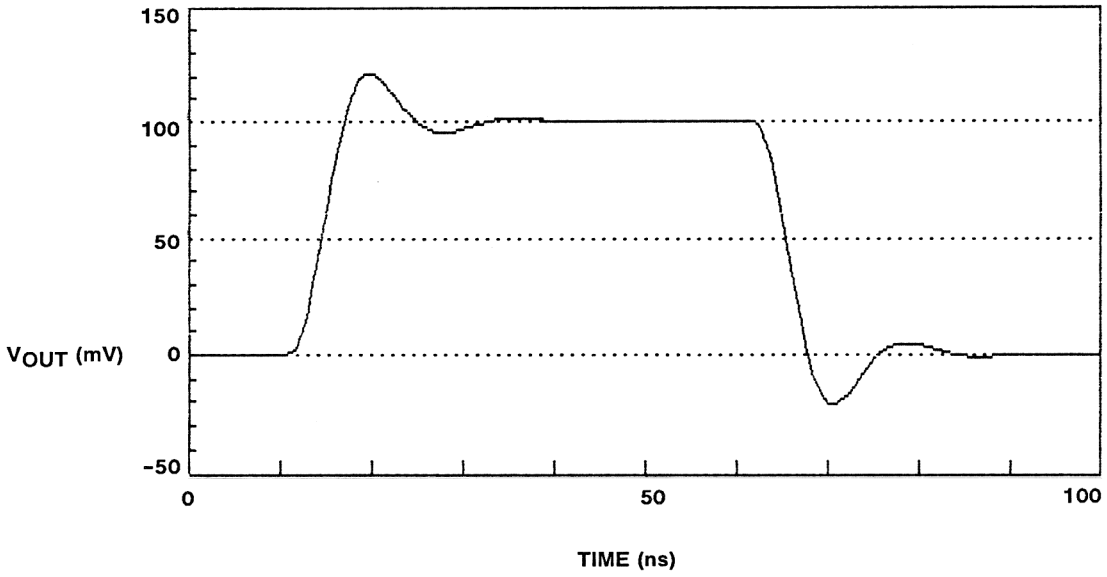


## Model Performance Conditions: $V_{SUPPLY}$ = ±15V, $A_{VCL}$ = +1, Unless Otherwise Specified

OPEN LOOP GAIN AND PHASE vs FREQUENCY
($R_L$ = 1K, $C_L$ = 10pF)

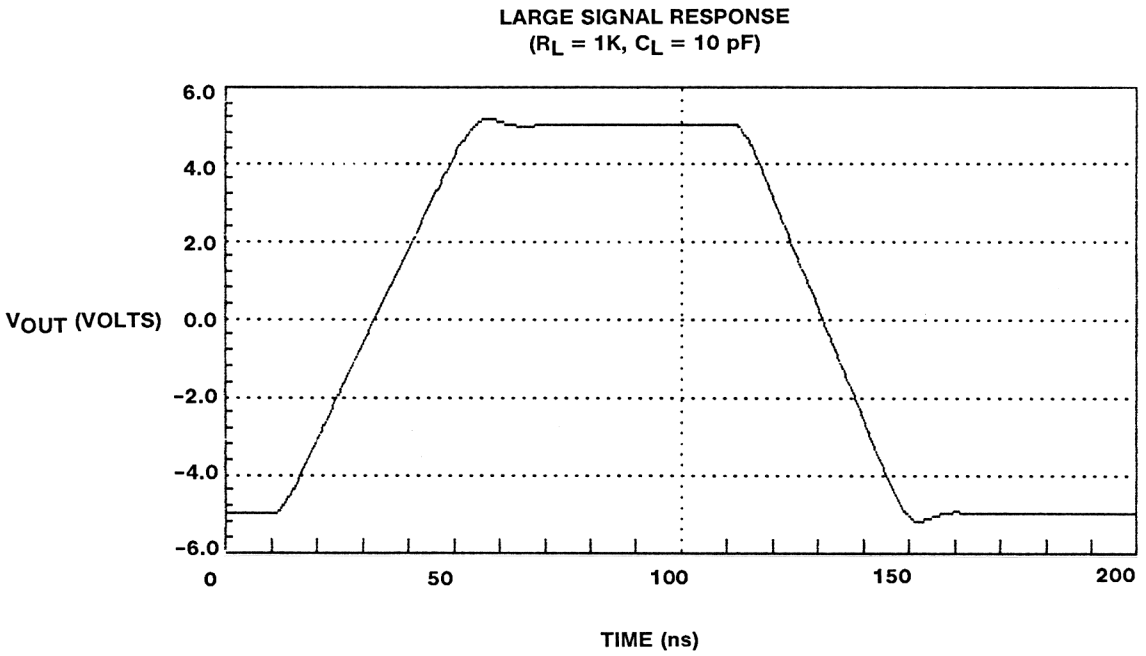



SMALL SIGNAL RESPONSE
($R_L$ = 1K, $C_L$ = 10pF)



## Model Performance (Continued)

Conditions $V_{SUPPLY}$ = ±15V, $A_{VCL}$ = +1, Unless Otherwise Specified



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